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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/756,961	01/13/2004	Yoshiyuki Shibata	10873.871USD1	4810

52835 7590 06/14/2006

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EXAMINER	
PHAM, HOAI V	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/756,961	SHIBATA, YOSHIYUKI	
	Examiner	Art Unit	
	Hoai v. Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-21* is/are pending in the application.

4a) Of the above claim(s) *9-15,18-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7,8,16,17 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/057,658.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action by sending a verified translation of application Serial No. JP2001-033445 is persuasive and, therefore, the finality of that action is withdrawn.

2. The new finality of the rejection is hereby below.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 7 is rejected under 35 U.S.C. 102(e) as being anticipated by DeBoer et al. [U.S. Pat. 6,737,696] newly cited.

DeBoer et al. (figs. 2, 5-17, cols. 2-6) discloses a method for manufacturing a semiconductor memory device comprising:

depositing an interlayer insulating film (142, 148) on a semiconductor substrate (112) provided with contact plugs (146) (see fig. 9);

pattering a mask pattern (not shown) on the interlayer insulating film, the mask pattern having a layout in which a plurality of hole patterns having the same shape are arranged in a stagger manner so that side edges of the adjacent hole patterns are only partially opposite to each other (see col. 4, lines 58-62);

forming holes (150) for storage nodes in the interlayer insulating film by etching with the mask pattern (see fig. 9);

forming the storage nodes (152) in the holes so as to be connected electrically to the contact plugs (see fig. 10);

forming a capacitor insulating film (153, 155, 157) on the storage nodes (see figs. 11-15); and

forming a plate electrode (156) on the capacitor insulating film (see fig. 16).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 7-8, 16-17 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang [U.S. Pat. 6,617,631] previously applied, in view of DeBoer et al. [U.S. Pat. 6,737,696] newly cited.

With respect to claim 7, Huang (figs. 7-12, cols. 6-8) discloses a method for manufacturing a semiconductor memory device comprising:

depositing an interlayer insulating film (42) on a semiconductor substrate (10) provided with contact plugs (40) (see fig. 8 and col. 6, lines 61-65);

pattering a mask pattern (not shown) on the interlayer insulating film (see col. 7, lines 10-11);

forming holes (8) for storage nodes in the interlayer insulating film by etching with the mask pattern (see fig. 9 and col. 7, lines 7-13);

forming the storage nodes (44) in the holes so as to be connected electrically to the contact plugs (see figs. 10-11 and col. 7, lines 14-27);

forming a capacitor insulating film (46) on the storage nodes (see fig. 11 and col. 7, lines 29-42); and

forming a plate electrode (48) on the capacitor insulating film (see fig. 12 and col. 7, lines 44-52).

Huang fails to disclose the mask pattern having a layout in which a plurality of hole patterns having the same shape are arranged in a stagger manner so that side edges of the adjacent hole patterns are only partially opposite to each other.

However, DeBoer et al. discloses that the mask pattern having a layout in which a plurality of hole patterns having the same shape are arranged in a stagger manner so that side edges of the adjacent hole patterns are only partially opposite to each other (see fig. 2 and col. 2 lines 1-24). Therefore, it would have been obvious to one having ordinary skill in the art to incorporate the teaching of DeBoer et al. into the process of Huang in order to reduce the parasitic capacitance being generated between storage

node electrodes and also to increase density the bit line contacts are shared by neighboring DRAMS cells.

With respect to claims 8 and 17, Huang (col. 6, lines 61-65) discloses that a relative dielectric constant of the interlayer insulating film (silicon oxide including fluorine = fluorosilicate glass (FSG) is inherently smaller than that of a silicon oxide.

With respect to claim 16, Huang discloses that the interlayer insulating film (42) is fluorosilicate glass (FSG), wherein the fluorosilicate glass (FSG) is inherently having a relative dielectric constant of 3.5 or less (see Tsai et al. [U.S. Pat. 6,331,480], col. 3, lines 15-18 for an evidence).

With respect to claim 21, Huang and Lee et al. does not explicitly disclose the percent range of the set cell capacitance value as claimed by Applicant. However, the percent range would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Response to Arguments

7. Applicant's arguments with respect to claims 7-8, 16-17 and 21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

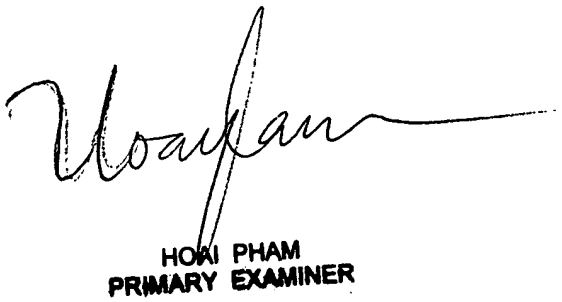
8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

9. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is 571-272-1715. The examiner can normally be reached on M-F.

11. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



HOAI PHAM
PRIMARY EXAMINER